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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,341	12/11/2003	Ming Yang Wang	FORT 2768	3753

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EXAMINER	
PATEL, SHAMBHAVI K	

ART UNIT	PAPER NUMBER
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/735,341	WANG ET AL.	
	Examiner	Art Unit	
	Shambhavi Patel	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/11/03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-29 are pending.

Specification

The attempt to incorporate subject matter into this application by reference to the application referred to on page 12 of the specifications is ineffective because no patent number for the reference is given.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

1. **Claim 27** is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

The examiner asserts that the current state of the claim language is such that a reasonable interpretation of the claims would not result in any concrete or tangible products. Merely determining whether or not to modify the netlist and whether or not a warning should be provided to the user does not produce a tangible output.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1, 14, and 27-29 are rejected** under 35 U.S.C. 102(b) as being clearly anticipated by **Selvidge (US Patent No. 6,009,531).**

As per **claims 1 and 14, Selvidge** is directed to a method for programming an emulator to emulate an integrated circuit (IC) described by a netlist as including logic blocks that communicate through synchronizing circuits, wherein the synchronizing circuits include input clock sinks for conveying input signals into logic blocks and output clock sinks for conveying output signals out of logic blocks (column 13 lines 31-65), and wherein the synchronizing circuits employ clock signals to clock the input and output clock sinks (figure 7B), the method comprising the steps of:

a. analyzing the netlist to determine a domain, a sub-domain and a phase of each clock signal each synchronizing circuit employs to clock its input and output clock sinks (column 11 lines 59-67). Selvidge discloses finding timing relationships between timing signals. Thus, relationships such as *phase-locked signals* (column 11 lines 29-40), non-simultaneous signals (column 11 lines 41-54), and asynchronous signals (column 11 lines

55-58) are determined. Selvidge also groups phase-clocked signals into *clock domains* and then determines the relationship between the domains.

b. analyzing the net list to determine a type of each synchronizing circuit based on relationships between the determined domain, sub-domain and phase of the clock signals the synchronizing circuit employs to clock its input and output signals (figure 19; column 11 lines 62-67). Selvidge discloses determining whether the signals are phase-locked (have identical or inverted phases), asynchronous, or non-simultaneous. The synchronizing circuit types comprise:

i. at least one type A synchronizing circuit wherein clock signals that clock the synchronizing circuit's input and output clock sinks are of similar domain, similar sub-domain and similar phase (column 8 lines 5-11). The synchronizer circuits share the VClk input clock signal (figure 8B), and thus have similar domain, subdomain, and phase.

ii. at least one type B synchronizing circuit wherein clock signals that clock the synchronizing circuit's input and output sinks are of similar domain, dissimilar subdomain, and similar phase (figure 9A). Object 910 have only one input clock signal, which is then processed to form the output signal. The output signal of object 910 then forms the input signal for object 912. Thus, the signals are of similar domain (both share CLK0), dissimilar subdomain (only object 912 has CLK1) and similar phase.

c. modifying the netlist description of each type B synchronizing circuit so that it becomes a type A synchronizing circuit (figure 19; column 9 lines 34-44). The new

circuit is controlled by synchronizers, which receive two clock signals as inputs, along with a common synchronized VClk signal, and output a control signal to the logic blocks. As per claim 14, the instructions are stored in an environment within the target system (figure 1; column 5 lines 56-64)

As per **claim 27**, Selvidge is directed to a method for programming an emulator to emulate an integrated circuit (IC) described by a netlist as including logic blocks that communicate through synchronizing circuits,

a. wherein the synchronizing circuits include input clock sinks for clocking input signals into logic blocks and output clock sinks, for clocking output signals out of logic blocks (*Selvidge*: column 13 lines 31-65)

b. wherein the input and output clock sinks are clocked by clock signals, wherein clock signals of the IC include at least one primary clock signal received as input to the IC and at least one secondary clock signal the IC derives from its at least one primary clock signal (*Selvidge*: figure 7B). There is one external clock fed into the system (ECLK) and this is passed through the synchronizer to form a clock synchronizer signal.

c. wherein the method comprises the steps of:

i. processing the netlist to identify classifications of clock signals within the IC, each primary clock signal being classified as being of a separate domain, each separately derived secondary clock signal being classified as being of the same domain and a separate sub-domain of each

primary clock signal from which it is derived (*Selvidge*: column 11 lines 27-59). Different timing relationships between the clock signals, such as phase-locked signals, asynchronous signals, and non-simultaneous signals are determined.

ii. processing the netlist to identify each synchronizing circuit and to ascertain its type based on relationships between the classifications of the clock signals it employs to clock its input and output clock sinks (*Selvidge*: column 11 lines 58-67)

iii. depending on the type of each synchronizing circuit type, determining whether the emulator will be able to successfully emulate the synchronizing circuit, whether to modify netlist description of the synchronizing circuit so that the emulator can emulate it (*Selvidge:* column 14 lines 47-67), and whether to provide a warning to the user that the synchronizing circuit is of a type that the emulator may not be able to emulate. It would be inherent to provide a warning to the user if the emulator is not able to emulate the circuit. Otherwise, the user will not be able to know whether or not the circuit operates correctly, thus defeating the purpose of using the emulator.

As per **claim 28**, Selvidge is directed to the method in accordance with claim 27 further comprising the step of modifying the netlist description of each synchronizing circuit determined at step c to be modified, thereby to produce a modified netlist (figure 19; column 20 lines 39-53).

As per **claim 29**, Selvidge is directed to claim 27 further comprising the step of programming the emulator to emulate an IC described by the modified netlist (figure 19; column 20 lines 39-53).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 1, 14, and 27-29** are rejected under 35 U.S.C. 102(e) as being anticipated by **Hyduke (US Patent No. 7,003,746).**

As per **claims 1 and 14, Hyduke** is directed to a method for programming an emulator to emulate an integrated circuit (IC) described by a netlist as including logic blocks that communicate through synchronizing circuits, wherein the synchronizing circuits include input clock sinks for conveying input signals into logic blocks and output clock sinks for conveying output signals out of logic blocks (column 6 lines 14-27), and wherein the synchronizing circuits employ clock signals to clock the input and output clock sinks (figure 3), the method comprising the steps of:

a. analyzing the netlist to determine a domain, and a sub-domain of each clock signal each synchronizing circuit employs to clock its input and output clock sinks (figure 2). The method disclosed by Hyduke involves finding all of the clocks, clock sources, the synchronous primitives with clock-driven inputs, and the clock domains of the netlist. Hyduke discloses a find clock domains subroutine that groups all synchronous primitives by their input clock signals (column 6 lines 57-60). A clock domain by definition is the part of the design that is driven by either a single clock or clocks that have constant phase relationships (i.e. a clock and its inverted clock).

b. analyzing the net list to determine a type of each synchronizing circuit based on relationships between the determined domain and sub-domain of the clock signals the synchronizing circuit employs to clock its input and output signals (column 6 lines 58-67), wherein synchronizing circuit types comprise:

i. at least one type A synchronizing circuit wherein clock signals that clock the synchronizing circuit's input and output clock sinks are of similar domain, and similar sub-domain (figure 5 primitive 82). Primitive 82 in figure 5 is synchronous, and acts as a clock source. It has only one input clock signal and one output clock signal. Thus, the two signals are of the same domain, sub-domain, and phase.

ii. at least one type B synchronizing circuit wherein clock signals that clock the synchronizing circuit's input and output sinks are of similar domain and dissimilar subdomain (figure 5 primitives 80, 81, and 83; column 7 lines 36-52). Primitives 80, 81, and 83 have two different input clock signals, and one output clock signal. Thus, they have similar domain and phase and dissimilar subdomain. To prevent

unexpected behavior that may arise from this time of circuit, Hyduke discloses replacing the original input signals with one clock enable input signal. Thus, there is one input clock signal and one output clock signal, and they have the same domain, subdomain, and phase.

c. modifying the netlist description of each type B synchronizing circuit so that it becomes a type A synchronizing circuit (column 7 lines 48-51). The primitives 80, 81,and 83 have been replaced with clock-enabled primitives.

As per claim 14, the instructions are stored in an environment within the target system (figure 1; column 4 lines 53-67)

As per **claim 27**, Hyduke is directed to a method for programming an emulator to emulate an integrated circuit (IC) described by a netlist as including logic blocks that communicate through synchronizing circuits,

a. wherein the synchronizing circuits include input clock sinks for clocking input signals into logic blocks and output clock sinks, for clocking output signals out of logic blocks (column 6 lines 14-27)

b. wherein the input and output clock sinks are clocked by clock signals, wherein clock signals of the IC include at least one primary clock signal received as input to the IC and at least one secondary clock signal the IC derives from its at least one primary clock signal (*Hyduke:* figure 3). There is one external clock signal (i.e. primary clock signal) and this is used to form a secondary clock signal (54)

c. wherein the method comprises the steps of:

i. processing the netlist to identify classifications of clock signals within the IC, each primary clock signal being classified as being of a separate domain, each separately derived secondary clock signal being classified as being of the same domain and a separate sub-domain of each primary clock signal from which it is derived (*Hyduke:* column 8 lines 26-67). The clock domains routine finds all clock sources (primary signals) and all primitives and synchronous primitives.

ii. processing the netlist to identify each synchronizing circuit and to ascertain its type based on relationships between the classifications of the clock signals it employs to clock its input and output clock sinks (column 8 lines 27-35)

iii. depending on the type of each synchronizing circuit type, determining whether the emulator will be able to successfully emulate the synchronizing circuit, whether to modify netlist description of the synchronizing circuit so that the emulator can emulate it (*Hyduke:* column 9 lines 21-24), and whether to provide a warning to the user that the synchronizing circuit is of a type that the emulator may not be able to emulate. A skilled artisan would recognize that it is necessary to provide a warning to the user if the simulator is not able to emulate the circuit. Otherwise, the user will not be able to know whether or not the circuit operates correctly, thus defeating the purpose of using the emulator.

As per **claim 28**, Hyduke is directed to the method in accordance with claim 27 further comprising the step of modifying the netlist description of each synchronizing circuit determined at step c to be modified, thereby to produce a modified netlist (column 7 lines 49-52).

As per **claim 29**, Hyduke is directed to claim 27 further comprising the step of programming the emulator to emulate an IC described by the modified netlist (column 10 lines 51-67)

Allowable Subject Matter

Claims 2-13, and 15-26, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art fails to disclose any of the following circuit types:

i. Type C synchronizing circuit (similar domain, dissimilar sub-domain, dissimilar phase)

ii. Type D synchronizing circuit (similar domain, similar sub-domain, dissimilar phase)

iii. Type E synchronizing circuit (dissimilar domains)

iv. Type F synchronizing circuit (at least one of the clock signals that clock the synchronizing circuit's input and output sinks is derived from more than one primary clock signal)

v. Type G synchronizing circuit (similar domain, similar sub-domain, mixed phase)

vi. Type H synchronizing circuit (similar domain, dissimilar sub-domain, mixed phase)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shambhavi Patel whose telephone number is (571) 272-5877. The examiner can normally be reached on Monday-Friday, 8:00 am – 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-2279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SKP

KAMINI SHAH
SUPERVISORY PATENT EXAMINER